

Figure 2 - Clock generator with desired clock rate/duty cycle using a high frequency oscillator/clock input.

Change the duty cycle of the clock to eliminate or suppress the nth-order harmonic of that clock (step 12).

Generate a low-interference clock having the changed duty cycle while keeping the predetermined frequency (step 14)

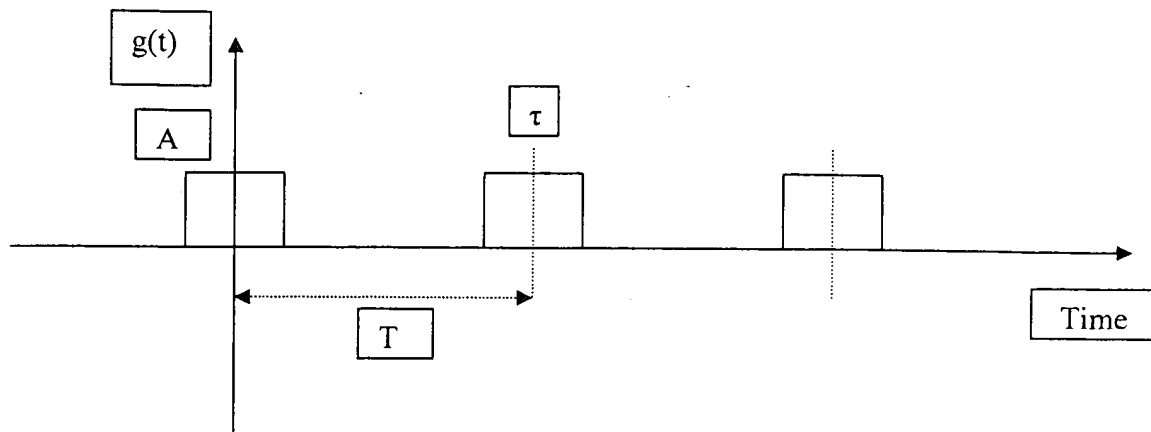
FIG. 3

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$$g(t) = A, \quad -\tau/2 \leq t \leq \tau/2$$

$$= 0, \quad \text{For the remainder of the period } T$$

Figure 1 – Exemplary square wave signal

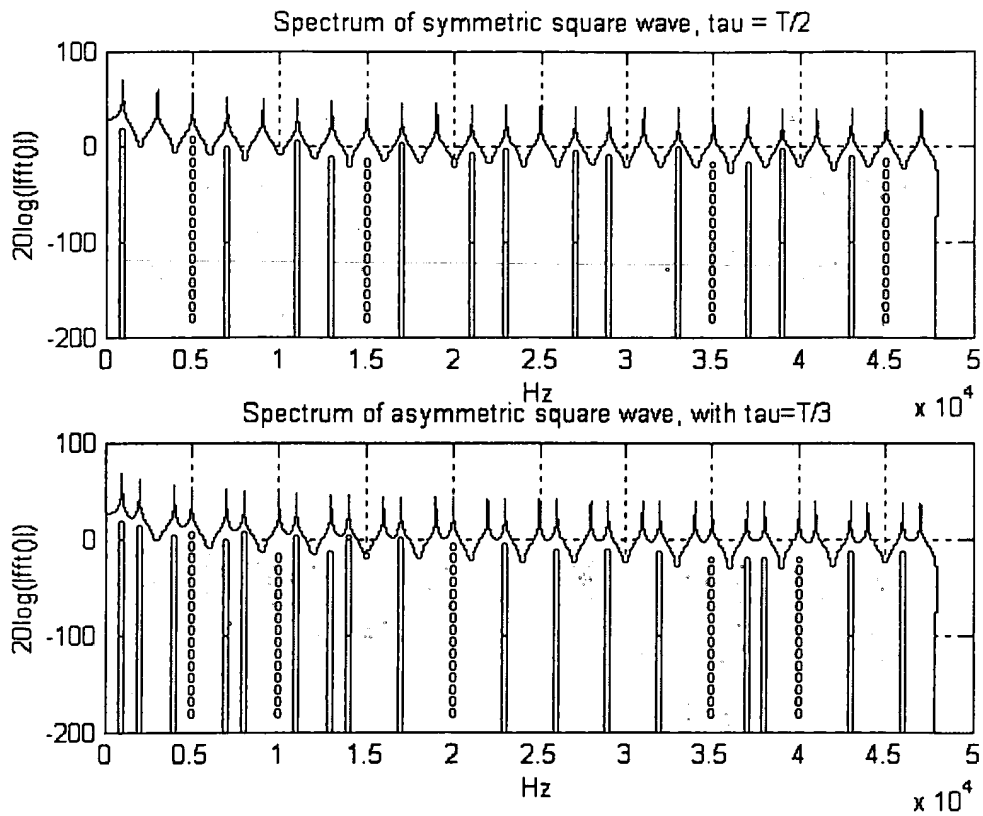


Figure 4 - Power Spectrum for a 1KHz clock (symmetric/asymmetric)

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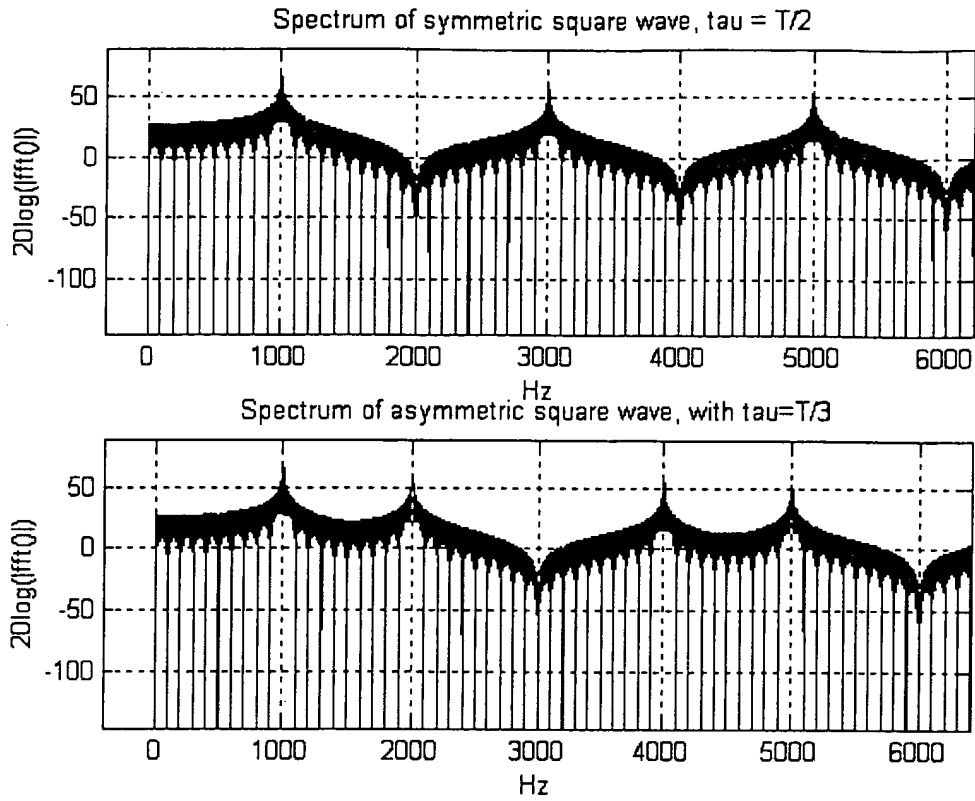


Figure 5 - Power Spectrum for the 1KHz clock (symmetric/asymmetric)

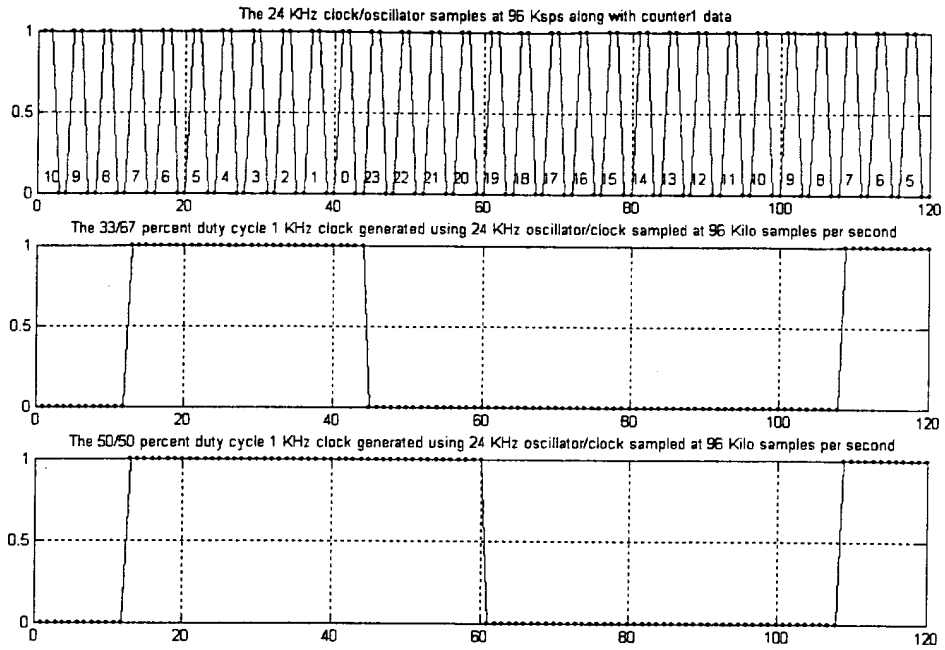


Figure 6 - Time domain analysis of the 24 KHz clock along with the 1KHz clock with different duty cycles.

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